



NSS – RADAR Signal Emulator Core

Version 1.5

Targeted Applications

- ELINT algorithm development & testing
- MIMO RADAR system designs
- VHF band LPI RADARs
- FPGA based BITE for RADAR signals

Product overview

The NSS Radar signal emulator (NSSRSE) product is FPGA based core for generating the digital RADAR signal both in baseband or IF band type. The core allows the user to select various parameters on the PC controlled GUI and changes the signal in FPGA dynamically. The NSSRSE is capable of generating various types of LPI signals including linear FM chirp, nonlinear FM chirp, and phase coding types.

The core is capable of generating multiple RADAR scenario signals with several parameters controllable through PC GUI. The PC can communicate with FPGA core by UART serial communication. The core can emulate all practical signal conditions such as AWGN and effective RADAR cross-section of the target with user selectable parameters. The product is shipped with optional hardware unit by which any FPGA board can be used for instantiating this core and testing the user function.

This core is ideal choice for RADAR related algorithm developer on FPGA platform, due its low cost and low area foot print on FPGA. The core is capable of running on any FPGA type occupying fewer resources.

Core Features

- → Linear FM or Non Linear FM selection
- → Upward or Downward chirp selection
- → barker codes (2.3.4.5.7.11 and 13 bit length)
- → Polyphase Frank code generation
- → Poly phase P1, P2, P3 and P4 code generation
- → Poly time T1,T2,T3 and T4 code generation
- → FSK based LPI signal generation
- Mixed FSK and PSK based LPI signal generation
- → Base band or IF level signal generation
- Programmable signal bandwidth up to 200 MHz
- → Simulated target based echo generation
- → Adjustable AWGN noise level
- Programmable RADAR cross section of the target
- → Pipelined architecture for high speed
- Optimized for FPGA implementation using block RAMs
- ◆ Supports all Xilinx FPGA types Spartan 3, 3E, 3A, 6, Virtex – 4, 5, 6
- → Synthesized netlist and wrapper VHDL files
- → Functionally equivalent MATLAB codes
- Chipscope drivers to further debug the results at different stages
- → User friendly GUI on PC
- → One year warranty
- → 6 months technical support over mail/web after product installation

Functional Block diagram

LPI configuration (LFM, Barker code) Power level, Frequency, PW, PRI No of signals Parameters of each Multi clock domain **BRAMs FPGA** Data buffering profile Controller **RADAR** signal gen-1 Signal combiner Serial cable **UART** (AWGN and **RADAR** core multipath effects) signal gen-2 Data formatter JTAG cable Target model (configurable RADAR target signal gen-N parameters) PC for profile creation using GUI echo Chipscope core Board settings (clk and FPGA type) User function or User function or algorithm Number of signals algorithm (ELINT) Parameters of each RADAR (RADAR) Speed limited by protocol Speed only limited by FPGA core clk

Ordering information

Part number: NSSRSE_1.5

CONTACT

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Other relevant links

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Wideband DDC http://nsscomm.com/wideband.html

DSP data compressor on FPGA http://www.nsscomm.com/dspdata.html

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